FPGA Implementation of Ternary Content Addressable Memory

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Abstract

Ternary Content Addressable Memories (TCAM) are the memories that search the data depend on the content stored in them. They are higher level than Content Addressable Memory (CAM) because they are search unknown value also i.e. ternary states, the ternary states is ternary-valued logic or multi-valued logic, in CAM we refer to memory that is addressable by binary data while in TCAM means that the data may contain “don’t care” bits besides logic zero and logic one values. TCAM is used in network routers, ATM switch systems ,data compression. This paper presents FPGA design and simulation to test a TCAM cell for its search operation using VHDL language with ISE9.2i program and implemented on FPGA Altera DE2 kit.

Keywords: TCAM ,VHDL, Field Programmable Gate Array (FPGA).

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1. Introduction

Network systems are continually called upon to support different applications in the network at line speed. Whether it is a classic problem such as IP-lookup, or an emerging domain such as worm detection, many network algorithms require the ability to index and search large amounts of state with incredibly high throughput. For example, in the case of IP-lookup, the state is a routing table, while for worm detection the state may be a set of patterns to match. While there is a great deal of work on advanced algorithms to speed the search through this state with traditional memories, the complexities of implementation motivate some to seek a memory design that directly supports the search primitives. Content Addressable Memories provide the required search capabilities with a minimum of additional cost and complexity[1].

Traditionally, digital computation is performed using two-valued logic, i.e., there are only two possible values (0 or 1, true or false) in the Boolean (binary) space. Multiple valued logic (MVL) has attracted considerable interest due to its potential advantages over binary logic for designing high performance digital systems . Theoretically, MVL has the potential of improving circuit performance for applications, such as arithmetic and digital signal processing. Compared to a binary design, a ternary logic (or three-valued logic) implementation requires fewer operations, less gates, and signal lines; hence, it is possible for ternary logic to achieve simplicity and energy efficiency in digital design, because this type of logic reduces the complexity of interconnects and chip area [2].

TCAM extends this functionality to include wildcard bits that will match both one and zero. These wildcards can be used on both the access operations of the memory (indicating some bits of the search are “don□t cares”).The fully parallel search provided by TCAM eases the implementation of many complex operations such as routing table lookup. Due to the fact that the TCAM searches every location in memory at once, the ordering of the elements in the TCAM is less important and large indexing structures can often times be entirely avoided. TCAM finds applications in other high-speed network operations such as packet classification, access list control, and pattern matching for intrusion detection[3] .

2 .TCAM architecture

General TCAM architecture consists of a core memory array, an address decoder, a comparand data driver, a bitline (BL) data driver, a searchline (SL) pre-discharger, a matchline (ML) precharger, ML sense amplifiers, and a priority logic encoder as shown in Fig (1),in a data searching operation, the search data is sent to the TCAM core to compare the comparand data with all the stored data simultaneously, and the address of the matched data is sent to the output if there is a match. In case multiple matches are found, the priority logic encoder prioritizes the addresses and sends the one with highest priority[4].

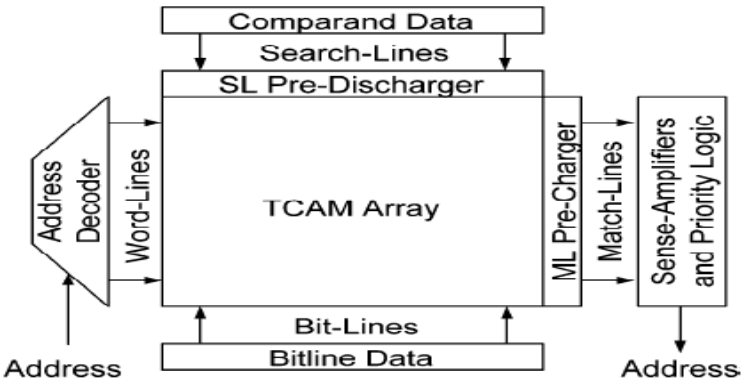
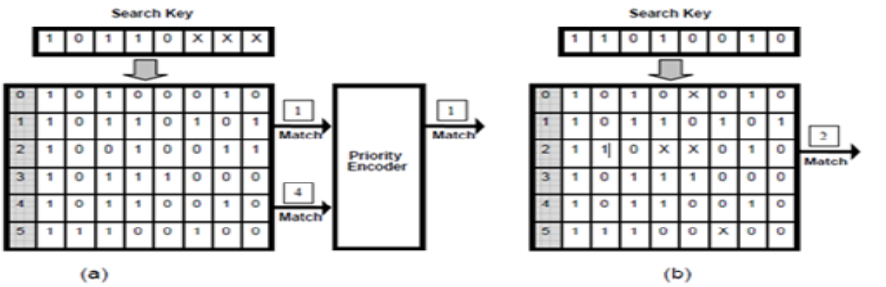


Fig (1) TCAM architecture

A more powerful and feature-rich TCAM can store and search ternary states (‘1’, ‘0’, and ‘X’). The state ‘X’, also called ‘mask’ or ‘don’t care’, can be used as a wild card entry to perform partial matching. Masking can be done both globally (in the search key) and locally (in the table entries). Fig(2) shows examples of global and local masking in TCAMs. The search key 10110XXX will match with all the entries that fall in the following range: 10110000 to 10110111 (words located at addresses 1 and 4 in this case). It is called global masking because the last three bits of all the table entries are ignored. In Fig(2-b), word 4 10-XX-010 (located at address 2) will match with any of the following search keys: 110-00- 010, 110-01-010, 110-10-010 and 110-11-010. The mask feature is particularly suitable for longest-prefix match searches in classless inter-domain routing (CIDR).

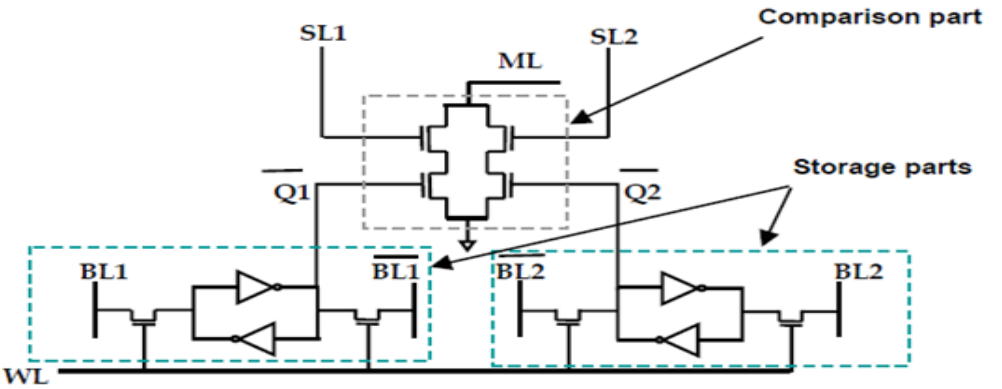
TCAMs are also becoming popular in solving other problems such as sorting and range searching[5].



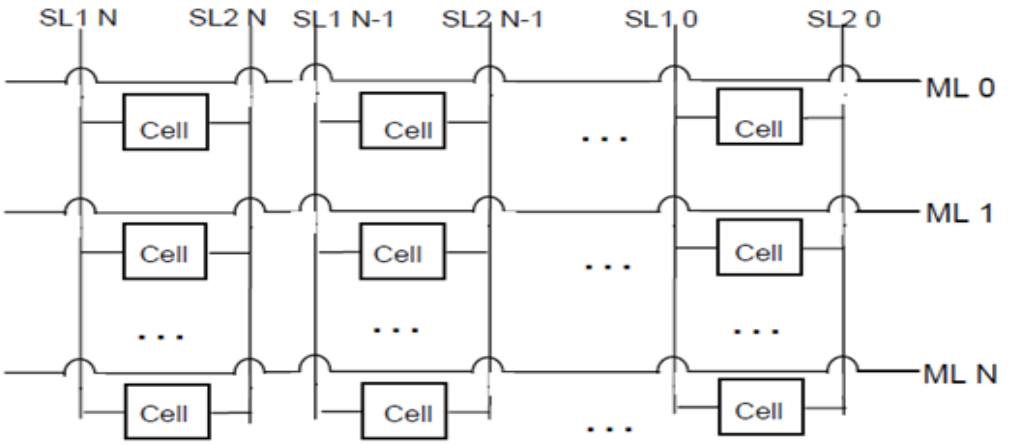
Fig(2) SEARCH operation in a TCAM with (a) global masking and (b) local masking

3.TCAM Cell

The biggest benefit of using a TCAM is that the comparison happens directly in the cells, which means that to understand the power consumed by the comparison operation we must understand the internals of a TCAM cell [3]. The high power consumption of TCAM is largely due to the comparison function used in the search operation. The TCAM cell consists of a storage circuit part and a comparison circuit part used in the search operation as shown in Fig(3). The TCAM core is implemented as an array of TCAM cells with horizontally running wordlines (WLs) and matchlines (MLs), and vertically running bitlines (BLs) and searchlines (SLs) as shown in Fig(4). All the cells in the same row share the same WLs and MLs, and all the cells in the same column share the same BLs and SLs[6].



Fig(3) Conventional TCAM Cell



Fig(4) TCAM Core

There are two types of cell in TCAM, the NOR and the NAND cells. Ternary cells, store an “X” value. The “X” value is a don’t care, that represents both “0” and “1”, allowing a wildcard operation. Wildcard operation means that an “X“ value stored in a cell causes a match regardless of the input bit. A ternary symbol can be encoded into two bits according to Table (1).

We represent these two bits as D and $\overline{D}$. Note that although D and $\overline{D}$ are not necessarily complementary. Since two bits can represent 4 possible states, but ternary storage requires only three states, we disallow the state where D and $\overline{D}$ are both zero. To store a ternary value in a NOR cell, we add a second SRAM cell, as shown in Fig(5). One bit, D, connects to the left pull down path and the other bit $\overline{D}$ connects to the right pull down path, making the pull down paths independently controlled. We store an "X" by setting both D and $\overline{D}$ equal to logic "1", which disables both, pull down paths and forces the cell to match regardless in the inputs. In addition to storing an "X", the cell allows searching for an "X" by setting both SL and $\overline{SL}$ to logic "0". This is an external don't care that forces a match of a bit regardless of the stored bit. The rest of the operations are listed in Table (1) and Table (2)[7].

Table(1)

TERNARY ENCODING FOR NOR CELL

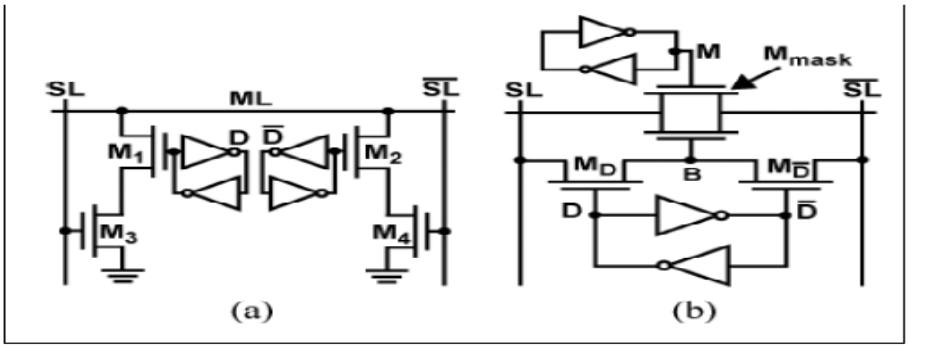
	Stored		Search Bit	
Stored Value	D	$\overline{D}$		
0	0	1	0	1
1	1	0	1	0
X	1	1	0	0

Table(2)

TERNARY ENCODING FOR NAND CELL

	Stored		Search Bit	
Value	D	M	SL	$\overline{SL}$
0	0	0	0	1
1	1	0	1	0
X	0	1	1	1
X	1	1	1	1

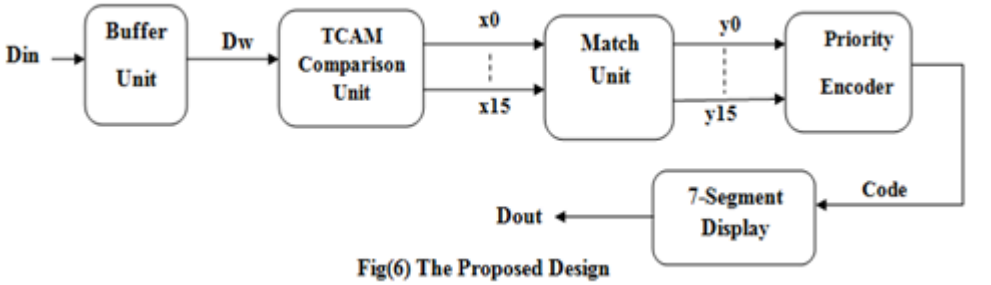
A NAND cell can be modified for ternary storage by adding storage for a mask bit at node M, as depicted in Fig. 5(b),when storing an "X", we set this mask bit, M mask, to "1". This forces transistor ON, regardless of the value of D, ensuring that the cell always matches. In addition to storing an "X", the cell allows searching for an "X" by setting both SL and $\overline{SL}$ to logic "1". Table (2) lists the stored encoding and search-bit encoding for the ternary NAND cell [8].



Fig(5) (a) NOR-type TCAM and (b) NAND-type TCAM

4. VHDL Simulation of The proposed design

The proposed design consists of five parts, the first part is the buffer unit in which it is used to store the desired value (8 bit digit) then it will transferred to the second part in which the data received will compared with all the words stored in the memory this part is name comparison unit,if there is any match words they will be appear (may be more than one) then these words will pass through a part called match unit in this unit these match words will separated and isolated to send to the priority encoder in which it will choose the desired word and send the line number of the row when data is found to light diodes and the value of the word will appear on a seven segment display, the proposed design is as shown below in Fig(6).



Fig(6) The Proposed Design

The proposed system built using vhdl language ,each part was checked alone to obtain the RTL scheme from the synthesis part of the vhdl

program and test electronically on test bench in the behavioral part ,all parts and there figures are listed as shown below:

1-The buffer unit: in this part the wanted data will received and passed to the comparison part, the RTL cct. and the test bench is as shown in Fig(7) &Fig(8):

Fig(7)RTL Circuit of Buffer

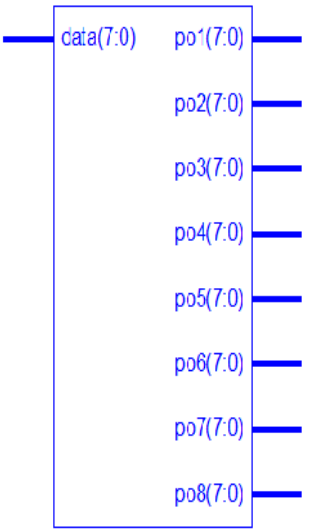
Fig(8)Test Bench of Buffer

2- The Comparison Unit: in this part the received word will compare with the available words in the memory as shown below in Table(3) to find its place, the RTL cct. and the test bench is as shown in Fig(9) &Fig(10).

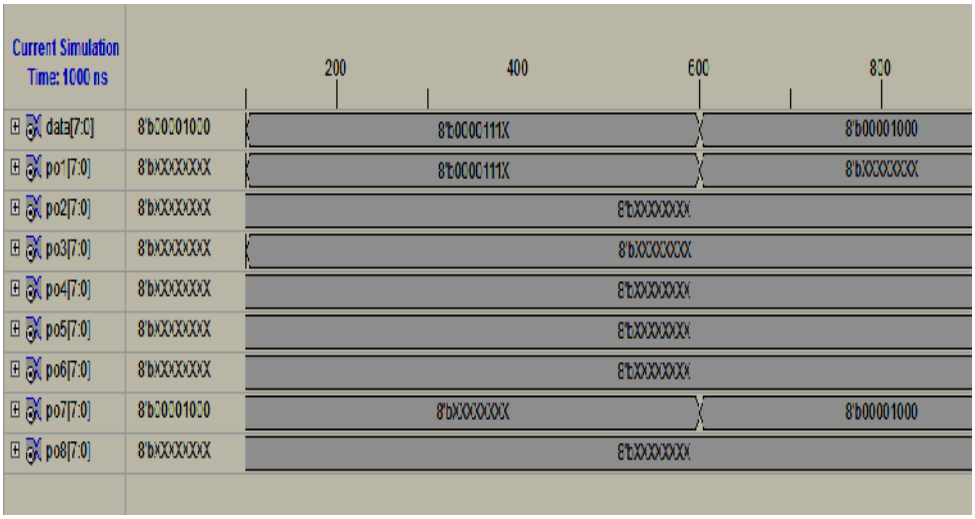
Table(3)

Words in the memory

No.	1	2	3	4	5	6	7	8
0	0	0	0	0	1	1	1	X
1	0	0	0	0	0	x	1	0
2	0	0	0	0	0	0	0	1
3	0	0	0	0	0	1	0	0
4	0	0	0	0	0	1	0	1
5	0	0	0	0	1	0	1	0
6	0	0	0	0	1	0	0	0
7	0	0	0	0	0	1	1	1

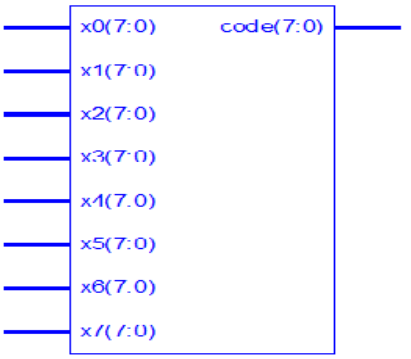


Fig(9)RTL Circuit of Comparison_unit



Fig(10)Test Bench of Comparison unit

3- The Match unit :in this part the desired word will appear may be more than one place then it will be collected to send it to the priority encoder part , the RTL cct. and the test bench is as shown in Fig(11) &Fig(12).



Fig(11) RTL Circuit of Match unit

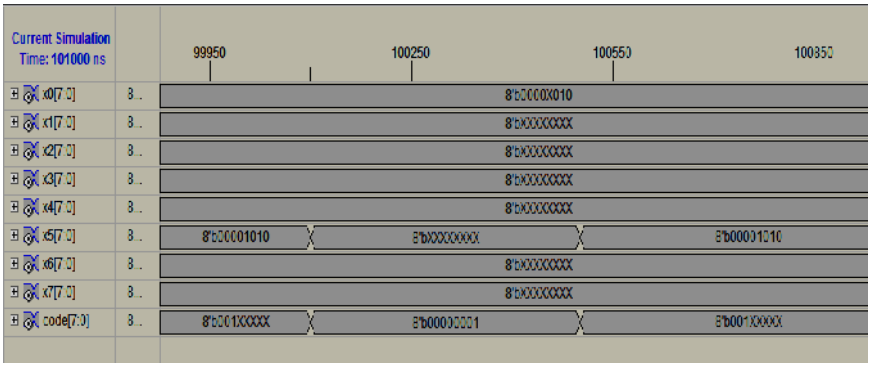


Fig (12) Test Bench of Match unit

4-The priority Encoder unit: this part is used when we have more than one match word ,it will choose the desired word according to table(4) shown

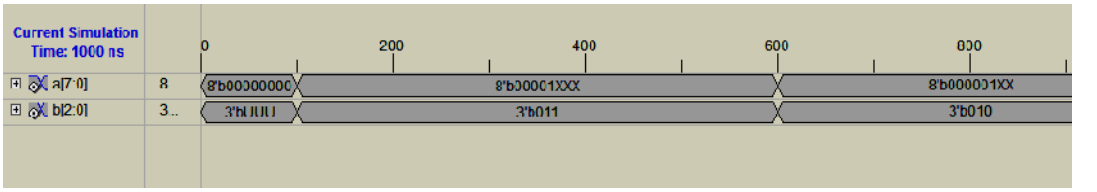
below and the RTL cct. and the test bench is as shown in Fig(13) &Fig(14).

Table(4)

Truth Table of Priority Encoder

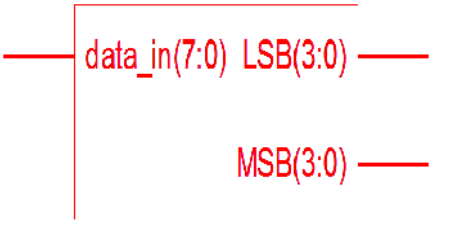
Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

Fig(13) RTL Circuit of of Priority Encoder

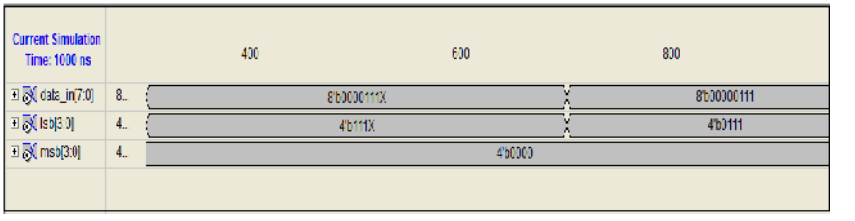


Fig(14)Test Bench of Priority Encoder

5-The Calling desired data unit : in this part the desired data will be send to a segment display after divided it into two parts as shown in the RTL cct. and the test bench in Fig(15) &Fig(16).

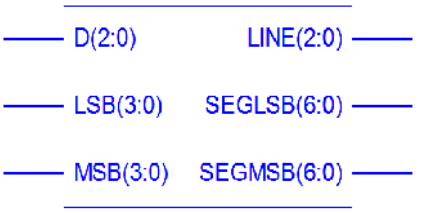


Fig(15) RTL Circuit of Calling data unit

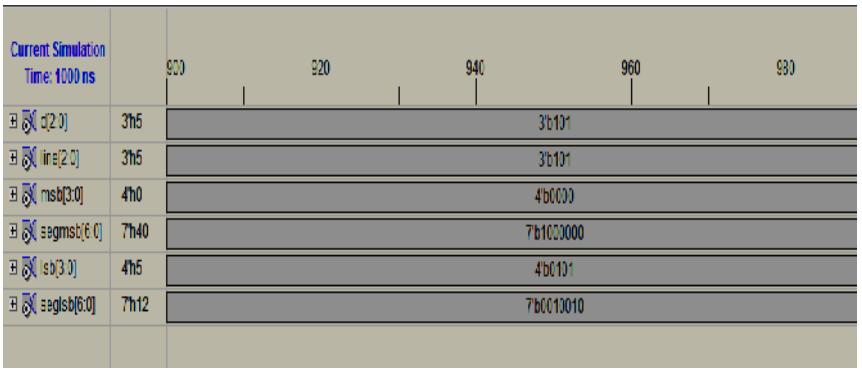


Fig(16)Test Bench of Calling data unit

6-The Display unit: in this unit the output of priority encoder and calling unit will pass through this circuit in order to display the final output that consists of the line in the memory rows and the data on it, the RTL cct. and the test bench in Fig(17) &Fig(18).

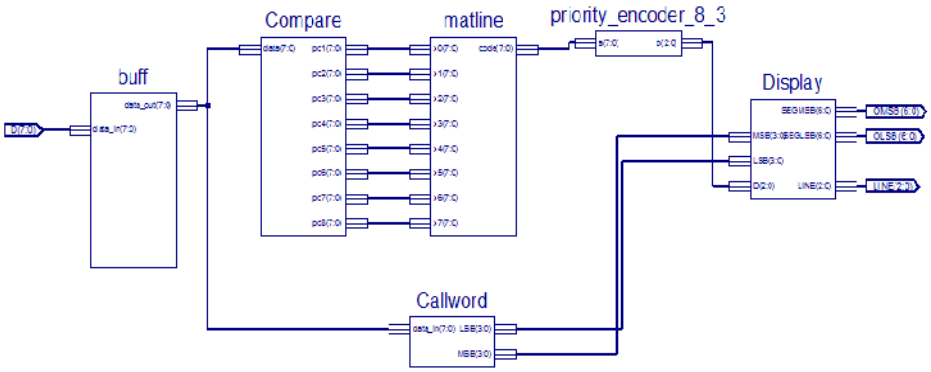


Fig(17) RTL Circuit of Display unit



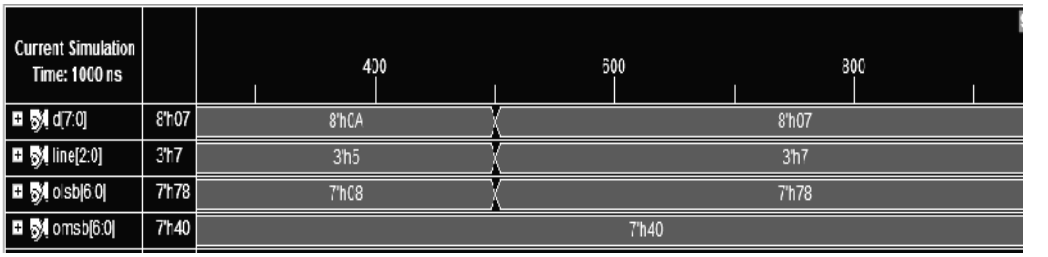
Fig(18)Test Bench of Display unit

After checking all the parts explained above, all these parts will be connected together using the facility of converting each vhdl program of the parts in the system into schematic circuit then connected them ,then test the connection between the parts to form the final design that contain all these parts as shown in Fig(19).



Fig(19) Overall Schematic Design

After checking the connection lines of the overall design ,then if it pass without errors ,we can again test its output as a complete circuit that contain the parts by supply the input to the buffer unit to see the output in the display unit as shown in Fig(20).



Fig(20)Test Bench of Complete Design

In fig(20) the test bench of the system will indicate that the input data applied to the buffer unit is denoted by d(7:0) with eight bit length the system will search on the memory then find its row in the memory as denoted by line(2:0) its mean three line because we have eight data words then the data will appear as least significant bit and most significant bit according to its status in the seven segment display as indicated in table (5) below.

The value of the output here explain the value of the seven segment display that represents the real value (according to the ALTERA DE2 Kit Applying a low logic level to a segment causes it to light up, and applying a high logic level turns it off, as shown below in Fig(21)

Fig(21) Value of Seven Segment Display

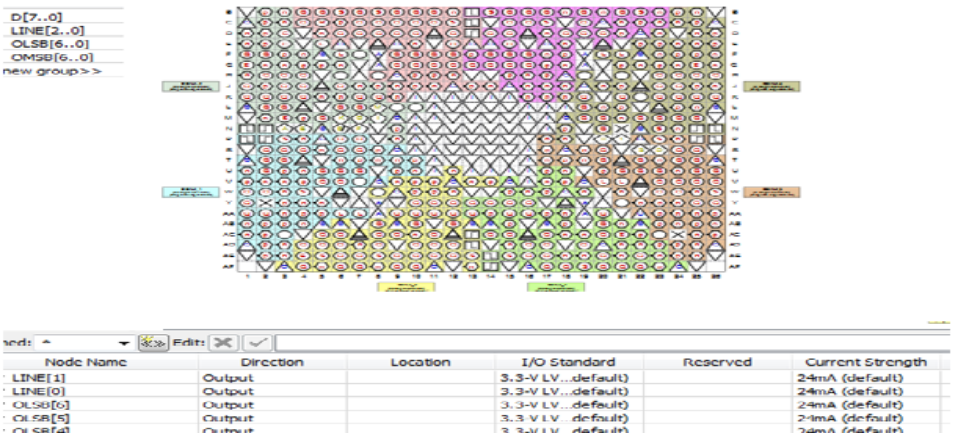
The seven segment values will be as shown in table (5):

Table(5).

No.	Digital value	Seven Segment Value(hex)
0	0000	40
1	0001	79
2	0010	24
3	0011	60
4	0100	19
5	0101	12
6	0110	02
7	0111	78
8	1000	00
9	1001	18
10	1010	08
11	1011	03
12	1100	46
13	1101	21
14	1110	06
15	1111	0E

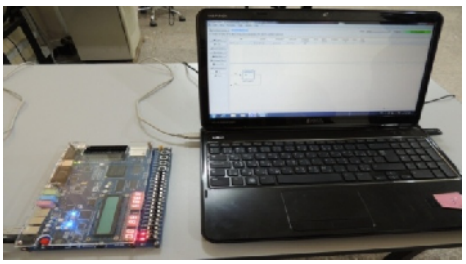
5.FPGA Implementation of TCAM:

After finish all the tests and checking of the final design ,we must take the vhdl program to implement it using the software of the ALTERADE2 Kit (QuartusII) ,then we need to convert the schematic circuit to a vhdl program, this will done using XILINX ISE9.2i program ,then copy the program to the Quartus program to check it after passing the check we must assign the inputs and the outputs of the circuit according to the kit, as shown in Fig(22):



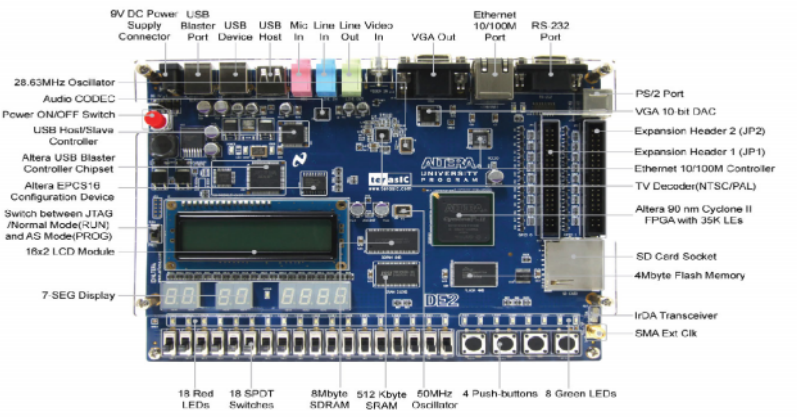
Fig(22) Assigning Input &Output of the the Kit

After assigning the input and output lines in the design according to kit ,check again after assigning to prepare the program to the kit for the implementation then programming as shown in Fig(23).



Fig(23) programming the Kit

The output of the implementation will appear when give input data of(8) bit from switches then see the row number on LEDs and the desired data on seven segment display(the Kit is as shown below in Fig (24),when search on one word we enter it from switches , the memory will give the line number of the row where the data is found and then the data found will appear on a seven segment display in the kit after we assign it to show the desired data as explained in Fig(25).



Fig(24)The Altera DE2 Kit

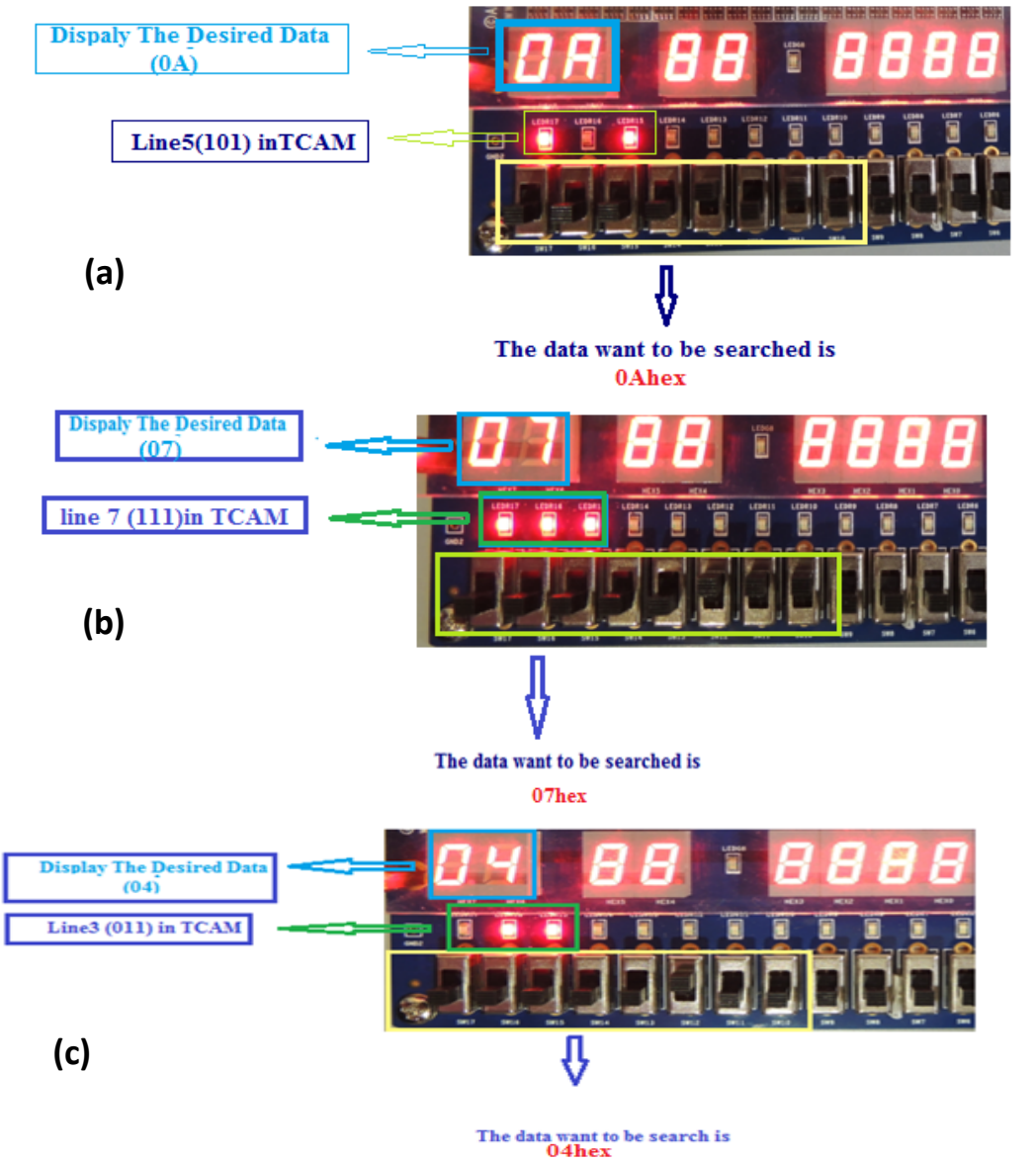


Figure (25) (a)Case (1) When Din=0Ahex (b)Case (2) When Din=07hex (c)Case (3) When Din=04hex

The content of TCAM is as shown below in table(6) ,the don't care is choose by the designer here chose zero value:

Table(6)

Content of TCAM

No.	1	2	3	4	5	6	7	8	Data
0	0	0	0	0	1	1	1	X	0E,0F
1	0	0	0	0	x	0	1	0	02 ,0A
2	0	0	0	0	0	0	0	1	01
3	0	0	0	0	0	1	0	0	04
4	0	0	0	0	0	1	0	1	05
5	0	0	0	0	1	0	1	0	0A
6	0	0	0	0	1	0	0	0	08
7	0	0	0	0	0	1	1	1	07

6.Conclusion : Ternary Content-Addressable Memories (TCAMs) are becoming popular for designing high-throughput forwarding engines on routers, in this paper a TCAM design provides a simple architecture and circuit, in which a don't-care data is used in the words of memory hierarchy and the search is done by comparing the wanted data with all the data stored. The benefit of using a FPGA Kit is the implementing of all the instructions concurrently this make FPGA IC very useful with this type of memory to increase it is speed in finding the wanted data .

7.References

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بناء ذاكرة محتوى العَنْوَنَة ثلاثية القيم باستخدام مصفوفة البوابات المنطقية المبرمجة

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المستخلص

ذاكرة محتوى العنونة ثلاثية القيم هي ذاكرة تقوم بالبحث عن البيانات بالاعتماد على المحتوى المخزون فيها، هي تعتبر اعلى مستوى من ذاكرة محتوى العنونه الثنائية القيم لانها تبحث عن القيم الغير معروفة قيمتها ايضا اي التي ليست صفر ولا واحد وتسمى ثلاثية القيم او متعددة القيم المنطقية . في ذاكرة محتوى العنونه العاديه او الثنائيه يتم الاشارة بالبحث عن البيانات ذات القيم الثنائيه المتعارف عليها وهي الـ (0,1) اما في ذاكرة محتوى العنونة الثلاثيه القيم سيتم اضافه قيمه ثالثه بالاضافه الى القيمتين اعلاه وهي قيمه غير محددة .هذا النوع من ذاكرة محتوى العنونه الثلاثية القيم يستخدم في مسارات الشبكات وفي انظمه تحويل نمط الانتقال الغير متزامن وفي ضغط البيانات . في هذا البحث نقدم تنفيذ عمليه بحث البيانات في خليه ذاكرة محتوى العنونة الثلاثي القيم باستخدام لغة وصف المكونات المادية باستخدام برنامج ISE9.2i ومن ثم تنفيذه على بطاقة مصفوفة البوابات المنطقية المبرمجة من نوع Altera DE2.

* الجامعة التكنولوجية