MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

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| **Module Information**  **معلومات المادة الدراسية** | | | | | | | | |
| **Module Title** | Logic circuits design | | | | | **Module Delivery** | | |
| **Module Type** | Core | | | | | * **☒ Theory** * **☐ Lecture** * **☒ Lab** * **☒ Tutorial** * **☒Practical** * **☐ Seminar** | | |
| **Module Code** | LOCD113 | | | | |
| **ECTS Credits** | 7 | | | | |
| **SWL (hr/sem)** | 175 | | | | |
| **Module Level** | | UGx11 1 | **Semester of Delivery** | | | | | 1 |
| **Administering Department** | | Type Dept. Code | **College** | | Type College Code | | | |
| **Module Leader** | [Mohammed Najm](https://ce.uotechnology.edu.iq/index.php/s/cv/921-mohammed-najm-abdullah-al-salam) | | **e-mail** | | mohammed.n.abdullah@uotechnology.ed.iq | | | |
| **Module Leader’s Acad. Title** | | Assistant Prof. | **Module Leader’s Qualification** | | | | | Ph.D. |
| **Module Tutor** | Dr.Rand Ali | | **e-mail** | [Rand.A.AbdulHussain@uotechnology.edu.iq](mailto:Rand.A.AbdulHussain@uotechnology.edu.iq) | | | | |
| **Peer Reviewer Name** | | 1. Dr. Dhari Ali 2. Lec. Noor Abdul Khaleq 3. Asst.Lect. Enas A. Raheem | **e-mail** | 1. [Dhari.a.mahmood@uotechnology.edu.iq](mailto:Dhari.a.mahmood@uotechnology.edu.iq) 2. [enas.a.raheem@uotechnology.edu.iq](mailto:enas.a.raheem@uotechnology.edu.iq) | | | | |
| **Scientific Committee Approval Date** | | 11/06/2023 | **Version Number** | | | | 1.0 | |

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| **Relation with other Modules**  **العلاقة مع المواد الدراسية الأخرى** | | | |
| **Prerequisite module** | None | **Semester** |  |
| **Co-requisites module** | None | **Semester** |  |

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| **Module Aims, Learning Outcomes and Indicative Contents**  **أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية** | |
| **Module Objectives**  **أهداف المادة الدراسية** | 1. To develop problem solving skills and understanding of logic circuit design methodology. 2. To familiarize students with the core ideas of Boolean algebra and how it is used in digital logic circuits. 3. The course deals with the basic concept of logic circuits. 4. The course is the building block for Computer Architecture course. 5. To understand how to design combinational logic circuits. 6. To understand and apply optimization algorithms to design logic circuits. |
| **Module Learning Outcomes**  **مخرجات التعلم للمادة الدراسية** | 1. Differentiate between analog and digital quantities. 2. Appreciate the power of using binary number system. 3. Realize the importance of digital codes. 4. Realize the importance of the abstraction provided by logic gates. 5. Use Boolean algebra to analyze and simplify logic circuits. 6. Use simulation of logic circuits. 7. Use Karnaugh map to optimize the Boolean expressions. 8. Grasp the concept of Don’t care and understand why Quine–McCluskey method is more suitable than Karnaugh map for simplifying more than four variables Boolean equations. 9. Apply systematic procedure to solve some of the digital design problems. 10. Utilize Verilog to verify the logic circuit design. 11. Understand universal gates properties and how to utilize these gates in the logic circuit implementation. 12. Understand how to implement arithmetic for computers. 13. Understand how to expand an existence design to solve bigger problems. 14. Understand how to reduce propagation delay. 15. Utilize algorithmic thinking to simplify the design of a digital system. |
| **Indicative Contents**  **المحتويات الإرشادية** | Indicative content includes the following:  Introduction to Digital Logic Design, Number Systems and Codes  Introduction to digital systems - Digital and analog quantities, binary digits, logic levels, digital waveforms, overview of basic logic functions, fixed-function integrated circuits, introduction to programmable logic, digital system application, positional number system, decimal numbers, binary numbers, number-base conversions, binary arithmetic, complements of numbers, signed binary numbers, arithmetic operation with signed binary numbers , hexadecimal numbers, octal numbers, binary coded decimal(BCD), digital codes. [6 hrs]  Logic Gates and Boolean Algebra  Review of AND, OR and NOT gates, NAND, NOR, EX-OR, EX-NOR, introduction to Hardware Description Languages (HDL), Boolean operation and expressions, laws and rules of Boolean algebra, De Morgan's Theorems, Boolean analysis of logic circuits, simplification using Boolean algebra, canonical and standard forms of Boolean expressions, Boolean expression and truth tables, developing Verilog model for logic circuits, gate delays, the Karnaugh Map, prime implicant and essential prime implicant, Karnaugh map minimization, don't care Conditions, Quine–McCluskey method. [10 hrs]  Combinational Logic Analyses  Basic combinational logic circuits, design procedure, implementing combinational logic, Verilog models of combinational logic circuits, code conversion, the universal property of NAND and NOR gates, Combinational logic using NAND gates only and NOR gates only. [6 hrs]  Combination Logic Circuit Applications  Half Adder, full Adder, half Subtractor, full Subtractor, parallel Binary adders and parallel Binary subtractors, 4-bit subtractor using 4-bit Adder, The Adder – Subtractor circuit, adder expansion, carry lookahead adder, decimal adder, parity generation and checking, magnitude comparator. [8 hrs] |

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| **Learning and Teaching Strategies**  **استراتيجيات التعلم والتعليم** | |
| **Strategies** | These learning and teaching strategies aim to create an engaging and interactive learning environment. We summarize them below:   1. **Lectures:** the instructor will present in-class lectures to introduce and clarify important concepts, theories, and principles related to the design of digital logic circuits. 2. **Interactive Discussions**: Engaging students in interactive discussions to encourage critical thinking. 3. **Hands-on Laboratory Work**: students gain practical experience in a controlled environment to reinforce theoretical concepts. 4. **Group Projects:** Assigning group projects that require students to collaborate and work together to solve logic circuit design problems. This promotes teamwork, communication, and division of tasks. 5. **Simulations and Virtual Labs**: Utilizing simulation software and virtual labs to provide students with virtual hands-on experiences when physical resources are limited. 6. **Use of Visuals and Multimedia:** Incorporating visual aids, multimedia resources, and interactive tools can enhance understanding and engagement. 7. **Assessment and Feedback**: Regular assessments, including quizzes, tests, and examinations to show how well the students understand the subject. 8. **Practice and Revision Sessions**: Providing dedicated practice sessions and revision classes enables them to improve students’ comprehension and strengthen their information. |

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| **Student Workload (SWL)**  **الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا** | | | |
| **Structured SWL (h/sem)**  **الحمل الدراسي المنتظم للطالب خلال الفصل** | 93 | **Structured SWL (h/w)**  **الحمل الدراسي المنتظم للطالب أسبوعيا** | 7 |
| **Unstructured SWL (h/sem)**  **الحمل الدراسي غير المنتظم للطالب خلال الفصل** | 57 | **Unstructured SWL (h/w)**  **الحمل الدراسي غير المنتظم للطالب أسبوعيا** | 6 |
| **Total SWL (h/sem)**  **الحمل الدراسي الكلي للطالب خلال الفصل** | **150** | | |

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| **Module Evaluation**  **تقييم المادة الدراسية** | | | | | |
| **As** | | **Time/Number** | **Weight (Marks)** | **Week Due** | **Relevant Learning Outcome** |
| **Formative assessment** | **Quizzes** | 2 | 10% (10) | 6 and 12 | LO #1- #5 and #6 - #11 |
| **Assignments** | 2 | 10% (10) | 3 and 12 | LO #2 and #5, #7, #11 |
| **Projects / Lab.** | 1 | 10% (10) | Continuous | All |
| **Report** | 1 | 10% (10) | 14 | LO #5 - #13 |
| **Summative assessment** | **Midterm Exam** | 2hr | 10% (10) | 8 | LO #1 - #7 |
| **Final Exam** | 3hr | 50% (50) | 16 | All |
| **Total assessment** | | | 100% (100 Marks) |  |  |

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| **Delivery Plan (Weekly Syllabus)**  **المنهاج الاسبوعي النظري** | |
| **Week** | **Material Covered** |
| **Week 1** | Introduction to digital and analog quantities, integrated circuits, and digital system applications |
| **Week 2** | Number-base conversions, binary arithmetic, octal and hexadecimal numbers, complements of numbers |
| **Week 3** | Signed numbers, arithmetic operation with signed binary numbers, BCD, digital codes |
| **Week 4** | Review of AND, OR and NOT gates, NAND, NOR, XOR, XNOR, introduction to Hardware HDL, Boolean operation and expressions, laws and rules of Boolean algebra, De Morgan's Theorems |
| **Week 5** | Boolean analysis of logic circuits, simplification using Boolean algebra, canonical and standard forms of Boolean expressions, Boolean expression, and truth tables |
| **Week 6** | developing Verilog model for logic circuits, gate delays |
| **Week 7** | Karnaugh Map, prime implicant and essential prime implicant, Karnaugh map minimization |
| **Week 8** | Midterm exam + don't care conditions, Quine–McCluskey method |
| **Week 9** | Basic combinational logic circuits, design procedure, implementing combinational logic |
| **Week 10** | Verilog models of combinational logic circuits, code conversion |
| **Week 11** | the universal property of NAND and NOR gates, Combinational logic using NAND gates only and NOR gates only |
| **Week 12** | Half Adder, full Adder, half Subtractor, full Subtractor |
| **Week 13** | parallel Binary adders and parallel Binary subtractors, 4-bit subtractor using 4-bit Adder, The Adder – Subtractor circuit, adder expansion |
| **Week 14** | carry lookahead adder, decimal adder |
| **Week 15** | Odd and Even functions, Parity generation and checking, magnitude comparator |
| **Week 16** | **Preparatory week before the final Exam** |

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| **Delivery Plan (Weekly Lab. Syllabus)**  **المنهاج الاسبوعي للمختبر** | |
| **Week** | **Material Covered** |
| **Week 1** | Lab 1: Introduction to the lab kits. |
| **Week 2** | Lab 2: NOT, AND, OR gates implementation using kit |
| **Week 3** | Lab 3: NAND, NOR, EX-OR, EX-NOR gates |
| **Week 4** | Lab 4: Rules of Boolean algebra (implementation using kit) |
| **Week 5** | Lab 5: Universal gates and De Morgan’s Theorems (implementation using kit) |
| **Week 6** | Lab 6: SOP (implementation using kit) |
| **Week 7** | Lab7: POS (implementation using kit) |
| **Week 8** | Lab 8: Karnaugh Map (implementation using kit) |
| **Week 9** | Lab 9: Karnaugh Map + don’t care condition (implementation using kit) |
| **Week 10** | Lab 10: Binary to Gray code, and Gray code to Binary (implementation using kit) |
| **Week 11** | Lab 11: BCD to Excess-3 Code Conversion (implementation using kit) |
| **Week 12** | Lab 12: Adders (implementation using Kit) |
| **Week 13** | Lab 13: Adders (implementation using Logisim) |
| **Week 14** | Lab 14: Subtractors (implementation using kit) |
| **Week 15** | Lab 15: Subtractors (implementation using Logisim) |

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| **Learning and Teaching Resources**  **مصادر التعلم والتدريس** | | |
|  | **Text** | **Available in the Library?** |
| **Required Texts** | 1-Digital Design with an Introduction to the Verilog, HDL, VHDL and System Verilog, Sixth edition, M. Morris Mano, Michael D. Ciletti, 2019.  2-Digital fundamentals, Eleventh Edition, Thomas L. Floyd, 2015. | NO  NO |
| **Recommended Texts** |  |  |
| **Websites** | https://www.coursera.org/learn/digital-systems | |

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| **Grading Scheme**  **مخطط الدرجات** | | | | |
| **Group** | **Grade** | **التقدير** | **Marks %** | **Definition** |
| **Success Group**  **(50 - 100)** | **A -** Excellent | **امتياز** | 90 - 100 | Outstanding Performance |
| **B -** Very Good | **جيد جدا** | 80 - 89 | Above average with some errors |
| **C -** Good | **جيد** | 70 - 79 | Sound work with notable errors |
| **D -** Satisfactory | **متوسط** | 60 - 69 | Fair but with major shortcomings |
| **E -** Sufficient | **مقبول** | 50 - 59 | Work meets minimum criteria |
| **Fail Group**  **(0 – 49)** | **FX –** Fail | **راسب (قيد المعالجة)** | (45-49) | More work required but credit awarded |
| **F –** Fail | **راسب** | (0-44) | Considerable amount of work required |
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| **Note:** Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above. | | | | |