MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

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| **Module Information**  **معلومات المادة الدراسية** | | | | | | | |
| **Module Title** | Digital Electronics | | | | **Module Delivery** | | |
| **Module Type** | S | | | | * **☒ Theory** * **☐ Lecture** * **☒ Lab** * **☒ Tutorial** * **☒ Practical** * **☐ Seminar** | | |
| **Module Code** | DIEL223 | | | |
| **ECTS Credits** | 6 | | | |
| **SWL (hr/sem)** | 150 | | | |
| **Module Level** | | UGx11 UG2 | **Semester of Delivery** | | | | 2 |
| **Administering Department** | | Type Dept. Code | **College** | Type College Code | | | |
| **Module Leader** | Dr. Ahmed Sabah Al-Araji | | **e-mail** | Ahmed.s.alaraji@uotechnology.edu.iq | | | |
| **Module Leader’s Acad. Title** | | Prof. | **Module Leader’s Qualification** | | | | Ph.D. |
| **Module Tutor** | Dr. Ahmed Sabah Al-Araji | | **e-mail** |  | | | |
| **Peer Reviewer Name** | | Name | **e-mail** | E-mail | | | |
| **Scientific Committee Approval Date** | |  | **Version Number** | | |  | |

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| **Relation with other Modules**  **العلاقة مع المواد الدراسية الأخرى** | | | |
| **Prerequisite module** | Electronic circuits | **Semester** |  |
| **Co-requisites module** | Electric circuits | **Semester** |  |

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| **Module Aims, Learning Outcomes and Indicative Contents**  **أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية** | |
| **Module Objectives**  **أهداف المادة الدراسية** | 1. Understanding basic concepts: Understanding the concepts of digital electronic circuit analysis and digital integrated circuit design and the practical applications of these concepts.  2. Application of techniques: The student’s ability to analyze problems and use the principles of transistor operation to solve them. Design models and program digital integrated circuits using advanced methods.  3. Data analysis: the ability to use scientific methods and electronic concepts in analyzing digital electronic circuits.  4. Improving performance: Learn how to analyze and design digital electronic circuits and use them to develop and improve the performance of integrated digital circuits. 5. Interaction with technology: developing the ability to deal with modern electronic technologies in the field of integrated digital electronic circuits and keeping pace with technological developments.  6. Creativity and innovation: encouraging students to use integrated digital electronic circuits creatively to solve problems and think in new ways.  7. Understanding complexity: Develop an understanding of complexity in the analysis and design of integrated digital electronic circuits and how to deal with it.  8. Teamwork: Enhancing teamwork skills through designs, projects, and challenges that require cooperation in teams.  9. Problem Solving: Improve problem solving and decision-making skills using advanced software techniques in analysis and design.  10. Evaluating and criticizing performance: The ability to evaluate the performance of models of designs for digital electronic circuits and improve them based on criticism and critical analysis. |
| **Module Learning Outcomes**  **مخرجات التعلم للمادة الدراسية** | 1. Providing practical models: Presenting practical examples and applications for using integrated electronic circuit technologies in various fields. This enables students to understand how to apply theoretical concepts to solve real-world problems through study, analysis, and design.  2. Practical projects: motivating students to implement practical projects that use programming techniques to analyze and design integrated digital electronic circuits, which helps in applying theoretical understanding and developing programming skills.  3. Solving case studies: providing case studies that address real challenges and problems that can be solved using integrated circuits. This encourages applied thinking and analysis of the complex problem.  4. Workshops and Discussions: organizing workshops and discussion sessions to encourage interaction and exchange of ideas among students. This enhances understanding of concepts and contributes to exchanging experiences, knowing the edge of scientific progress, and keeping pace with it.  5. Use of technology: using modern software and tools related to digital electronic circuits to provide interactive learning experiences and stimulate deep understanding.  6. Motivating self-research: encouraging students to conduct self-research on specific topics in the design of integrated digital electronic circuits, which enhances research and exploration skills.  7. Interactive evaluation: Using interactive evaluation techniques, such as providing feedback on individual or group projects, to promote continuous improvement.  8. Providing various resources: Providing various learning resources, such as explanatory videos, e-books, and articles, to meet the needs of different students.  9. Encouraging cooperative learning: organizing group learning activities where students cooperate to solve problems and exchange knowledge.  10. Stimulating innovation: encouraging students to develop new solutions and innovations in the field of digital electronics. |
| **Indicative Contents**  **المحتويات الإرشادية** | Indicative content includes the following.  Logic families explain the logic families based the integrated circuit such as Bipolar Logic Families Unipolar Logic Families, Saturated Logic Families, Non-saturated Logic Families, then explain the prosperities of the logic families such as Noise Margin, Propagation Delay Time, Switching Speed Limitations, Operating Temperature, Switching speed limitations, and Power Dissipation.  Design integrated circuit based on Resistor-Transistor Logic family, design OR gate, AND gate, Not gate, NAND gate, NOR gate and design Transistor-Transistor Logic Families based on OR gate, AND gate, Not gate, NAND gate, NOR gate, Open Collector TTL, and Tri-State TTL.  Analyze and design two different types of the operational amplifiers applications: linear applications and non-linear applications.  Design an oscillators and waveform generators with different IC are used.  Explain and design the ADC and DAC Converters. |

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| **Learning and Teaching Strategies**  **استراتيجيات التعلم والتعليم** | |
| **Strategies** | Teaching strategies adopted in digital electronic circuit analysis class and design circuit encourage students to stimulate their imagination in understanding digital electronic integrated circuits and component operations in different digital electronic systems. Also, help them to improve skills in discovering digital electronic integrated circuit. This will be achieved through classes, interactive tutorials and by considering types of simple experiments involving some sampling activities that are interesting to the students. |

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| **Student Workload (SWL)**  **الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا** | | | |
| **Structured SWL (h/sem)**  **الحمل الدراسي المنتظم للطالب خلال الفصل** | 93 | **Structured SWL (h/w)**  **الحمل الدراسي المنتظم للطالب أسبوعيا** | 6 |
| **Unstructured SWL (h/sem)**  **الحمل الدراسي غير المنتظم للطالب خلال الفصل** | 57 | **Unstructured SWL (h/w)**  **الحمل الدراسي غير المنتظم للطالب أسبوعيا** | 3 |
| **Total SWL (h/sem)**  **الحمل الدراسي الكلي للطالب خلال الفصل** | **150** | | |

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| **Module Evaluation**  **تقييم المادة الدراسية** | | | | | |
| **As** | | **Time/Number** | **Weight (Marks)** | **Week Due** | **Relevant Learning Outcome** |
| **Formative assessment** | **Quizzes** | 2 | 10% (10) | 5 and 10 | LO #1, #2 and #10, #11 |
| **Assignments** | 2 | 10% (10) | 2 and 12 | LO #3, #4 and #6, #7 |
| **Projects / Lab.** | 1 | 10% (10) | Continuous | All |
| **Report** | 1 | 10% (10) | 13 | LO #5, #8 and #10 |
| **Summative assessment** | **Midterm Exam** | 2hr | 10% (10) | 7 | LO #1 - #7 |
| **Final Exam** | 3hr | 50% (50) | 16 | All |
| **Total assessment** | | | 100% (100 Marks) |  |  |

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| **Delivery Plan (Weekly Syllabus)**  **المنهاج الاسبوعي النظري** | |
| **Week** | **Material Covered** |
| **Week 1** | * **Logic families** * Bipolar Logic Families * Unipolar Logic Families * Saturated Logic Families * Non-saturated Logic Families * Noise Margin, * Propagation Delay Time, * Switching Speed Limitations, * Operating Temperature, * Switching speed limitations, * Power Dissipation, |
| **Week 2** | * **Resistor-Transistor Logic IC Design** * OR gate, AND gate, Not gate, NAND gate, NOR gate * Diode-Transistor Logic IC Design * OR gate, AND gate, Not gate, NAND gate, NOR gate |
| **Week 3** | * Direct Coupled Transistor Logic * Integrated Injection Logic * High Threshold Logic |
| **Week 4** | * **Transistor-Transistor Logic Families** * OR gate, AND gate, Not gate, NAND gate, NOR gate * Open Collector TTL * Tri-State TTL |
| **Week 5** | * Fan-in Fan-out * Schottky Transistor Logic |
| **Week 6** | * **Complementary metal–oxide–semiconductor CMOS Logic Families** * OR gate, AND gate, Not gate, NAND gate, NOR gate * TTL to CMOS and CMOS to TTL Voltage Level |
| **Week 7** | * **Array Logic:** PAL, PLA, GAL, RAM ,Memory Decoding, SPD, CPLD |
| **Week 8** | * **Field Programmable Gate Arrays FPGA** |
| **Week 9** | * **Operational amplifiers.** * Introduction. Non-inverting Op-Amp. Inverting Op-Amp. * Voltage follower. |
| **Week 10** | * Voltage adder and subtractor. * Integrator. * Differentiator. |
| **Week 11** | * Current to Voltage Converter. * Voltage to Current Converter. * Electronics Analog Computation. |
| **Week 12** | * **Nonlinear Applications of Operational Amplifiers** * Comparator. * Window Comparator |
| **Week 13** | * Oscillators and Waveform Generators. * Timer 555 IC |
| **Week 14** | * **D/A converters.** * Resistive divider DAC. * Binary ladder DAC. * DAC accuracy and resolution |
| **Week 15** | * **A/D Converters.** * Simultaneous ADC. * Continuous ADC Single Slope and dual slope. * Counter-type ADC. * Successive approximation ADC * Flash ADC |
| **Week 16** | **Preparatory week before the final Exam** |

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| **Delivery Plan (Weekly Lab. Syllabus)**  **المنهاج الاسبوعي للمختبر** | |
| **Week** | **Material Covered** |
| **Week 1** | Characteristics of TTL Gates (Totem-Pole Output) – Part 1 |
| **Week 2** | Characteristics of TTL Gates (Totem-Pole Output) – Part 2 |
| **Week 3** | Characteristics of open collector TTL gates – Part 1 |
| **Week 4** | Characteristics of open collector TTL gates – Part 2 |
| **Week 5** | Characteristics of tri-state TTL gates – **Part 1** |
| **Week 6** | Characteristics of tri-state TTL gates – **Part 2** |
| **Week 7** | Introduction to OP-AMP Amplifier (OP-AMP) – **Part 1** |
| **Week** | Introduction to OP-AMP Amplifier (OP-AMP) – **Part 2** |
| **Week 9** | **Inverting** and **Non-Inverting** Operational Amplifier (OPAMP)– **Part 1** |
| **Week 10** | **Inverting** and **Non-Inverting** Operational Amplifier (OPAMP)– **Part 2** |
| **Week 11** | IC Timer-Based Multivibrators –**Part 1** |
| **Week12** | IC Timer-Based Multivibrators – **Part 2** |
| **Week13** | The Monostable multivibrator –**Part 1** |
| **Week14** | The Monostable multivibrator –**Part 2** |
| **Week15** | ALU arithmetic logic unit |

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| **Learning and Teaching Resources**  **مصادر التعلم والتدريس** | | |
|  | **Text** | **Available in the Library?** |
| **Required Texts** | Shiv Shanker "Digital Circuit and Systems II ", 2009 | Yes |
| **Recommended Texts** | M. Morris Mano "Digital Design" 4th edition , 2007 | yes |
| **Websites** |  | |

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| **Grading Scheme**  **مخطط الدرجات** | | | | |
| **Group** | **Grade** | **التقدير** | **Marks %** | **Definition** |
| **Success Group**  **(50 - 100)** | **A -** Excellent | **امتياز** | 90 - 100 | Outstanding Performance |
| **B -** Very Good | **جيد جدا** | 80 - 89 | Above average with some errors |
| **C -** Good | **جيد** | 70 - 79 | Sound work with notable errors |
| **D -** Satisfactory | **متوسط** | 60 - 69 | Fair but with major shortcomings |
| **E -** Sufficient | **مقبول** | 50 - 59 | Work meets minimum criteria |
| **Fail Group**  **(0 – 49)** | **FX –** Fail | **راسب (قيد المعالجة)** | (45-49) | More work required but credit awarded |
| **F –** Fail | **راسب** | (0-44) | Considerable amount of work required |
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| **Note:** Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above. | | | | |