Ministry of Higher Education and Scientific Research - Iraq
Al-Mansour University College
Department of Communication Engineering

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Digital Techniques**			**Module Delivery**	
Module Type	**Core**			☒ Theory ☐ Lecture ☒ Lab ☐ Tutorial ☐ Practical ☐ Seminar	
Module Code	**COM 11103**				
ECTS Credits	**7**				
SWL (hr/sem)	**175**				
Module Level	**UGI**	**Semester of Delivery**	**1**		
Administering Department	**BSc – COMM**	**College**	**Al-Mansour University College**		
Module Leader		**e-mail**			
Module Leader's Acad. Title		**Module Leader's Qualification**			
Module Tutor		**e-mail**			
Peer Reviewer Name		**e-mail**			
Scientific Committee Approval Date	**12/06/2023**	**Version Number**	**1.0**		

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	

Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	1. To acquire the basic knowledge of Digital techniques levels and application of knowledge to understand digital electronics circuits. 2. Have a thorough understanding of the fundamental concepts and techniques used in digital electronics 3. To understand and examine the structure of various number systems and its application in digital design. 4. The ability to understand, analyze and design various combinational and sequential circuits. 5. Ability to identify basic requirements for a design application and propose a cost effective solution. 6. To prepare students to perform the analysis and design of various digital electronic circuits.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	Important: Write at least 6 Learning Outcomes, better to be equal to the number of study weeks. 1. express basic concepts and logic circuits 2. Explains number systems and convert number systems. 3. explains logical AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR functions 4. can show the simplification of logical statements 5. explains the simplification of logical statements with using Boolean rules and de-Morgan theorems 6. Writes Boolean equation by using truth table and shows its logic circuits. 7. Writes Boolean equation by logic circuits and shows its truth table. 8. explains the simplification of logical statements with Karnaugh maps. 9. identifies 10. explains half and full adders 11. explains half and full subtractors 12. identifies combinational circuit 13. explains the working principles of decoder, encoder,

	14. recognize 7-segmented displayers 15. explains the working principles of multiplexer and De multiplexer, 16. shows the applications of combinational circuits
Indicative Contents المحتويات الإرشادية	Indicative content includes the following. Part A – number system and simplification of digital circuit design. **Introduction to digital quantities and System Numbers:** Decimal, Binary, Binary arithmetic, Octal and Hexadecimal Numbers, Conversions of System Numbers, Arithmetic Operations with different number systems, and Signed Numbers. [24 hrs.] **Digital Codes**: Binary coded decimal [BCD], Exc-3 code, Gray codes. [5 hrs.] **Simplification of digital circuit design:** Boolean algebra, De 'Morgan theorems, Simplification Using Boolean Algebra, Standard Forms of Boolean Expressions (SOP and POS form), The Karnaugh Map (Three, Four and Five-Variable Karnaugh Maps. [25 hrs.] Part B - Combinational Logic **Functions of Combinational Logic:** Adders, Subtracters, Parallel Binary Adders, multiplier, and Magnitude comparators. [25 hrs.]. Encoders, Decoders, Multiplexers, Demultiplexers, Parity Generators /Checkers, and code conversion circuits [25 hrs.]. **Flip-Flops:** Latches, Edge-Triggered Flip-Flops and its applications. [5 hrs.].

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering types of simple experiments involving some sampling activities that are interesting to the students.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ 15 اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	**93**	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	**6.2**
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	**82**	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	**5.5**
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**175**		

Module Evaluation
تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	2	10% (10)	5 and 10	LO #1, #2 and #10, #11
	Assignments	2	10% (10)	2 and 12	LO #3, #4 and #6, #7
	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	13	LO #5, #8 and #10
Summative assessment	Midterm Exam	2hr	10% (10)	7	LO #1 - #7
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)
المنهاج الاسبوعي النظري

	Material Covered
Week 1	Introduction to Digital Techniques and logic gates, General number formula : Binary, octal, decimal, hexadecimal numbers
Week 2	Conversions of System Numbers

Week 3	Arithmetic operations with different number systems, complements of number systems, binary codes, BCD codes, Ex-3 code, and gray code.
Week 4	Boolean algebra, De' Morgan theorems, Simplification Using Boolean Algebra
Week 5	Standard Forms of Boolean Expressions (SOP and POS form)
Week 6	The Karnaugh Map (two, Three, Four and Five- Variable Karnaugh Maps)
Week 7	Introduction to Combinational Logic circuit and circuit analysis
Week 8	Adders, Subtractors, Parallel Binary Adders,
Week 9	Binary multiplier circuits and Magnitude comparators circuit.
Week 10	Flip-Flops:(Latches, Edge-Triggered Flip-Flops) and it's applications.
Week 11	Counter and Shift register
Week 12	Encoders, and Decoders circuits
Week 13	Multiplexers, and Demultiplexers circuits.
Week 14	Parity Generators/Checkers and design of code conversion circuits.
Week 15	Analogue to Digital convertor and Digital to Analogue convertor
Week 16	**Preparatory week before the final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Introduction to logic gates
Week 2	Lab 2: NOR Gate, NAND Gate, and XOR Gate application
Week 3	Lab 3: Comparator Circuit
Week 4	Lab 4: Half –Adder
Week 5	Lab 5: full –Adder Circuit
Week 6	Lab 6: Half Subtractor

Week 7	Lab 7: full Subtractor Circuit
Week 8	Lab 8: Even and odd Parity Generator and Checker Circuit
Week 9	Lab 9: Code converter Circuits
Week 10	Lab 10: Encoder Circuit
Week 11	Lab 11: Decoder Circuit
Week 12	Lab 12: Multiplexer Circuit
Week 13	Lab 13: De - Multiplexer Circuit.
Week 14	Lab 14: Flip- Flop application Circuits
Week 15	Lab 15: Counter circuit
Week 16	Preparatory week before the final Exam

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	**Available in the Library?**
Required Texts	Digital Fundamentals, Thomas. L. Floyd, Pearson international edition.	Yes
Recommended Texts	Digital Design, M. Morris. Mano, Pearson prentice Hall.	No
Websites		

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks %**	**Definition**
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.